OIPE JC174 JAN 06 2004 PATENT & TRADEMARK OFFICE

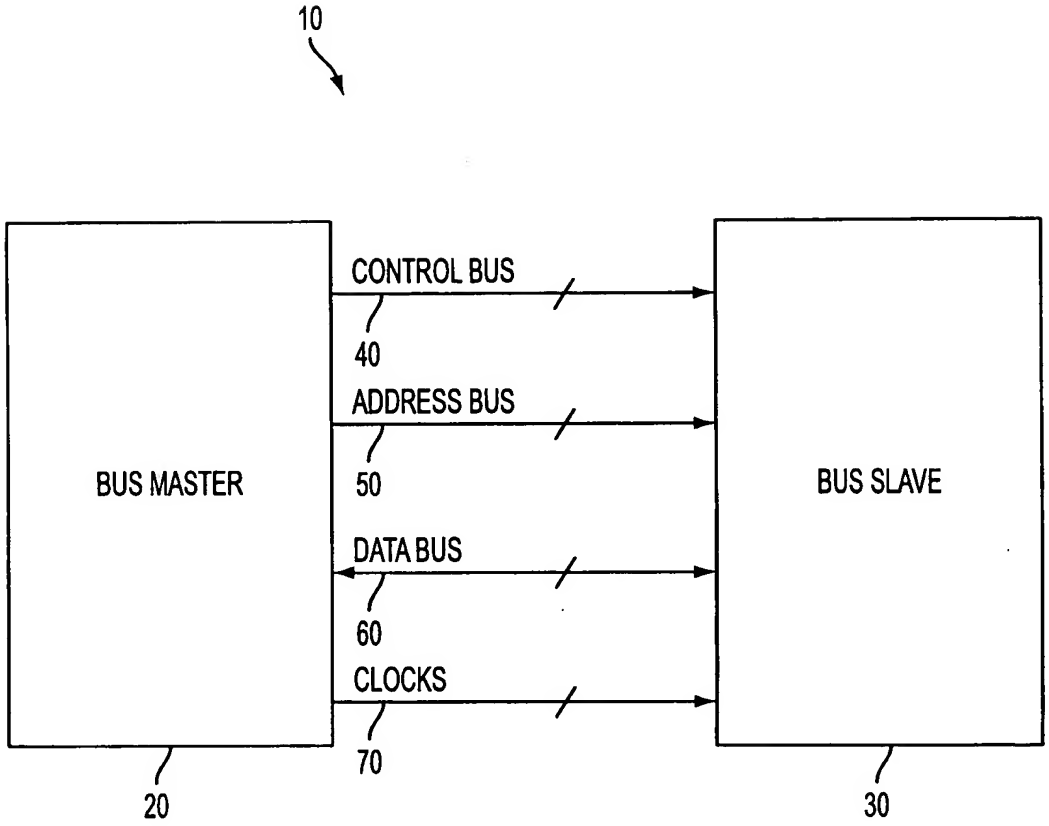

FIG. 1

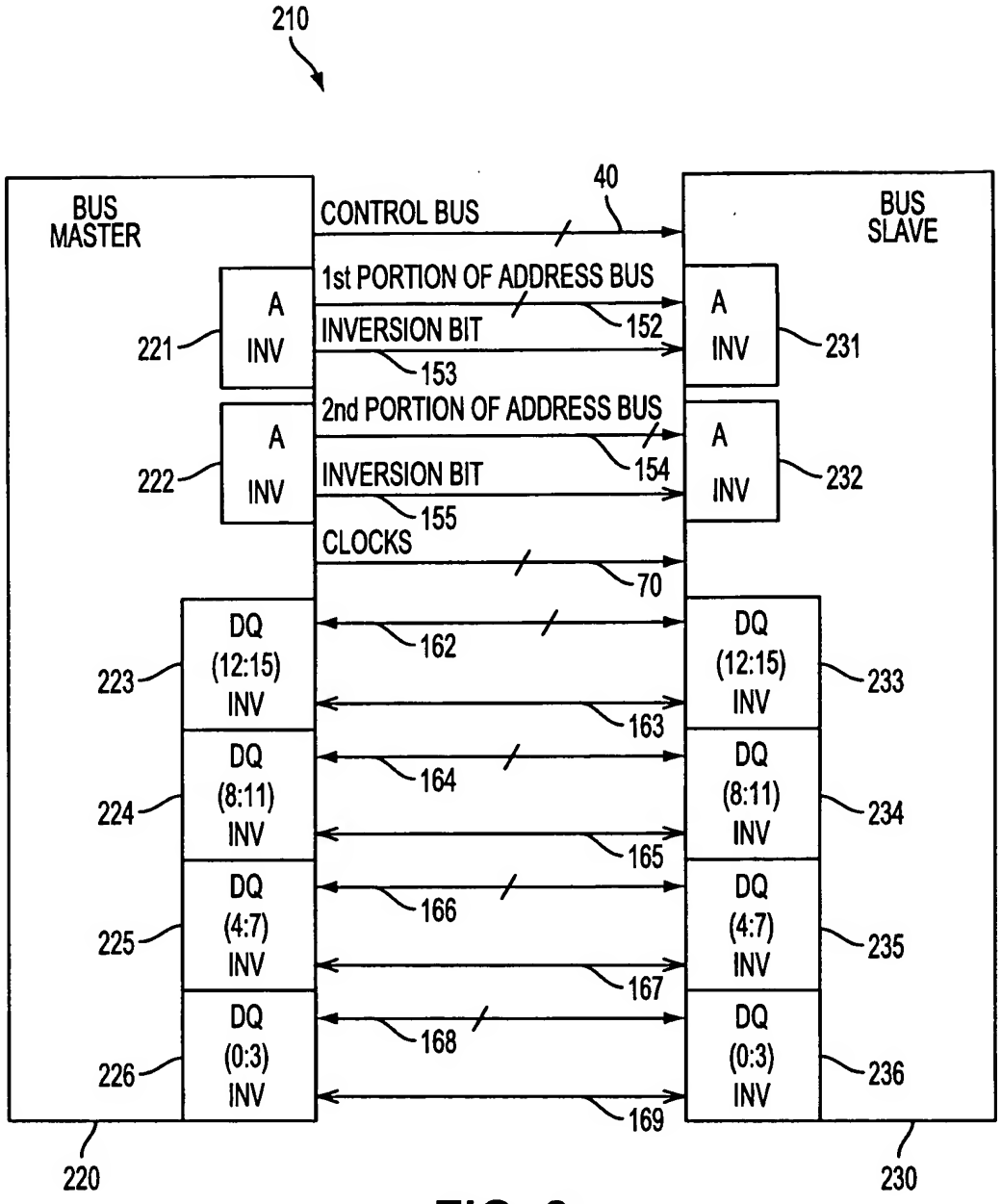
210
BUS MASTER
CONTROL BUS
40
BUS SLAVE
1st PORTION OF ADDRESS BUS
A INV
221
INVERSION BIT
152
153
A INV
231
2nd PORTION OF ADDRESS BUS
A INV
222
INVERSION BIT
154
155
A INV
232
CLOCKS
70
DQ (12:15) INV
223
162
163
DQ (12:15) INV
233
DQ (8:11) INV
224
164
165
DQ (8:11) INV
234
DQ (4:7) INV
225
166
167
DQ (4:7) INV
235
DQ (0:3) INV
226
168
169
DQ (0:3) INV
236
220
230

FIG. 2

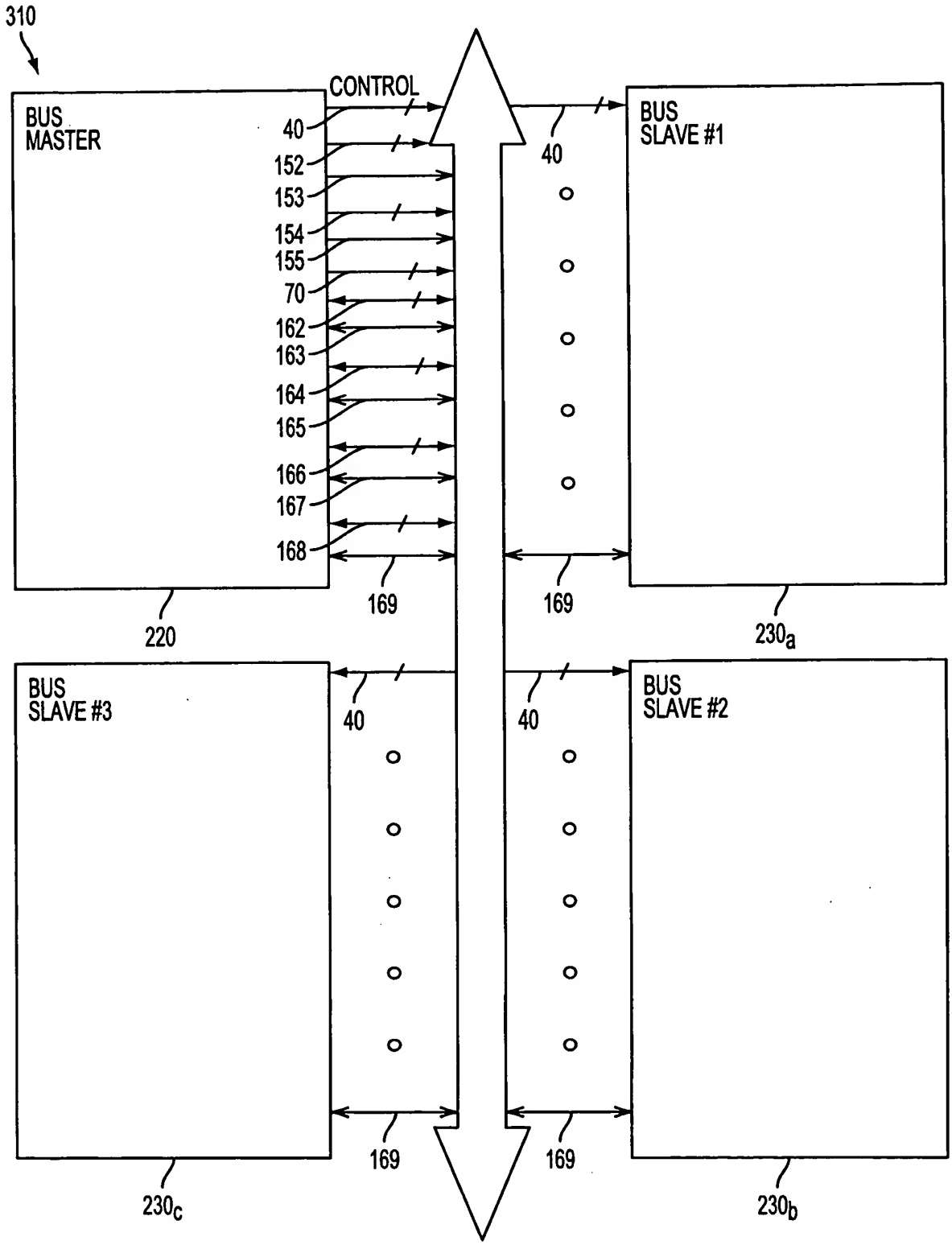
310
BUS MASTER
CONTROL
40
152
153
154
155
70
162
163
164
165
166
167
168
169
220
BUS SLAVE #1
40
169
230a
BUS SLAVE #3
40
169
230c
BUS SLAVE #2
40
169
230b

FIG. 3

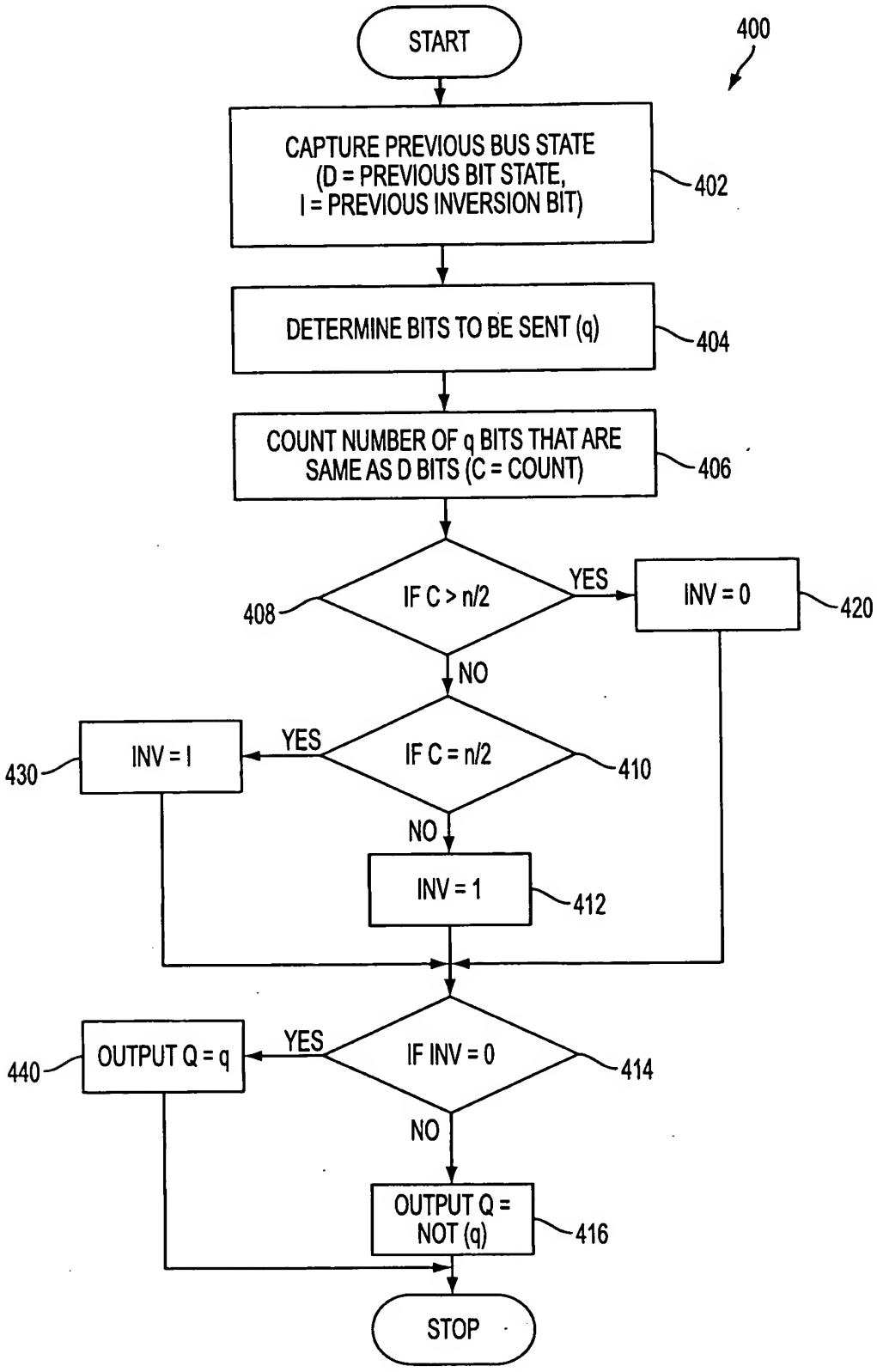
START
400
CAPTURE PREVIOUS BUS STATE (D = PREVIOUS BIT STATE, I = PREVIOUS INVERSION BIT)
402
DETERMINE BITS TO BE SENT (q)
404
COUNT NUMBER OF q BITS THAT ARE SAME AS D BITS (C = COUNT)
406
IF C > n/2
408
YES
INV = 0
420
NO
IF C = n/2
410
YES
INV = I
430
NO
INV = 1
412
IF INV = 0
414
YES
OUTPUT Q = q
440
NO
OUTPUT Q = NOT (q)
416
STOP

FIG. 4

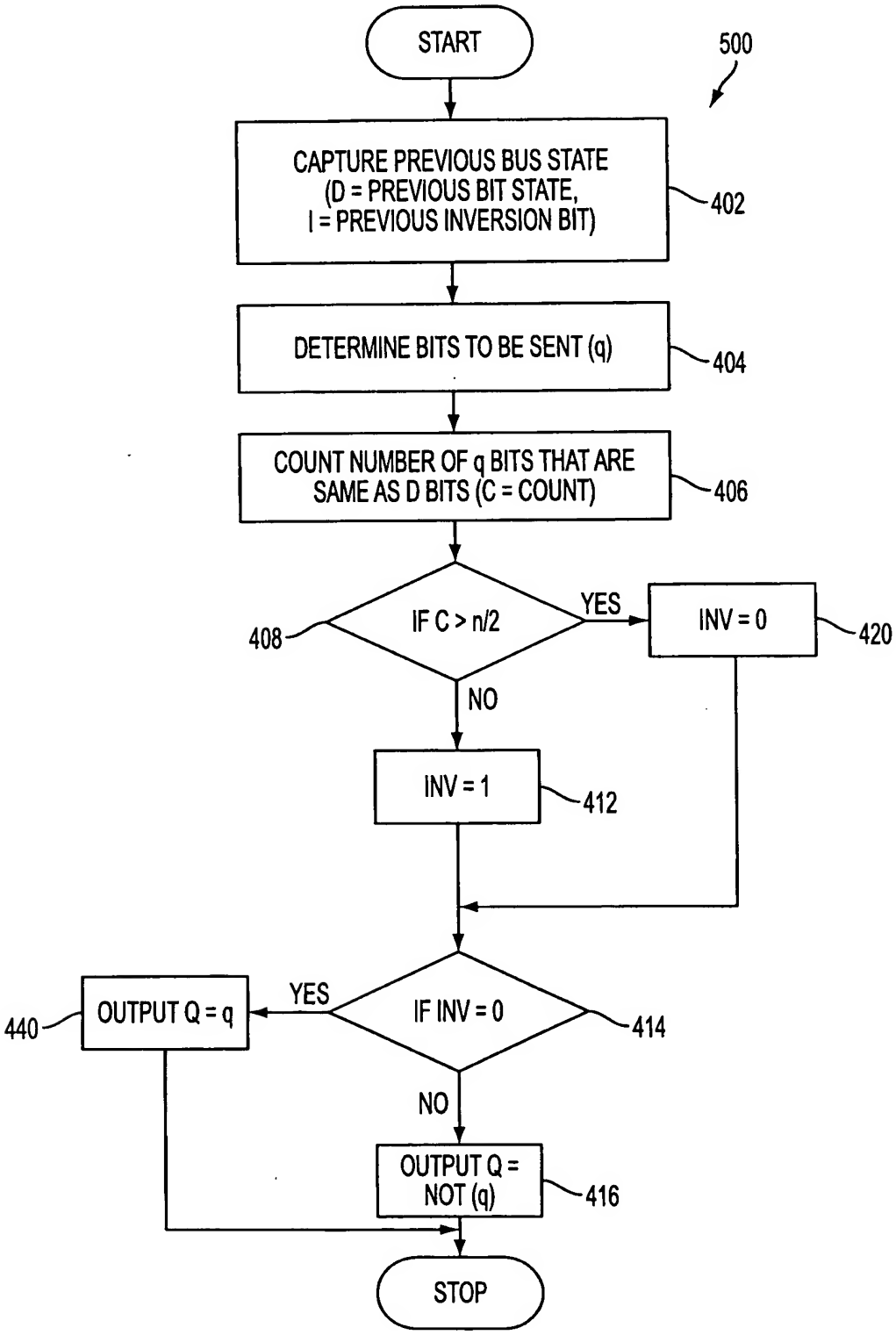
START
500
CAPTURE PREVIOUS BUS STATE (D = PREVIOUS BIT STATE, I = PREVIOUS INVERSION BIT)
402
DETERMINE BITS TO BE SENT (q)
404
COUNT NUMBER OF q BITS THAT ARE SAME AS D BITS (C = COUNT)
406
IF C > n/2
408
YES
INV = 0
420
NO
INV = 1
412
IF INV = 0
414
YES
OUTPUT Q = q
440
NO
OUTPUT Q = NOT (q)
416
STOP

FIG. 5

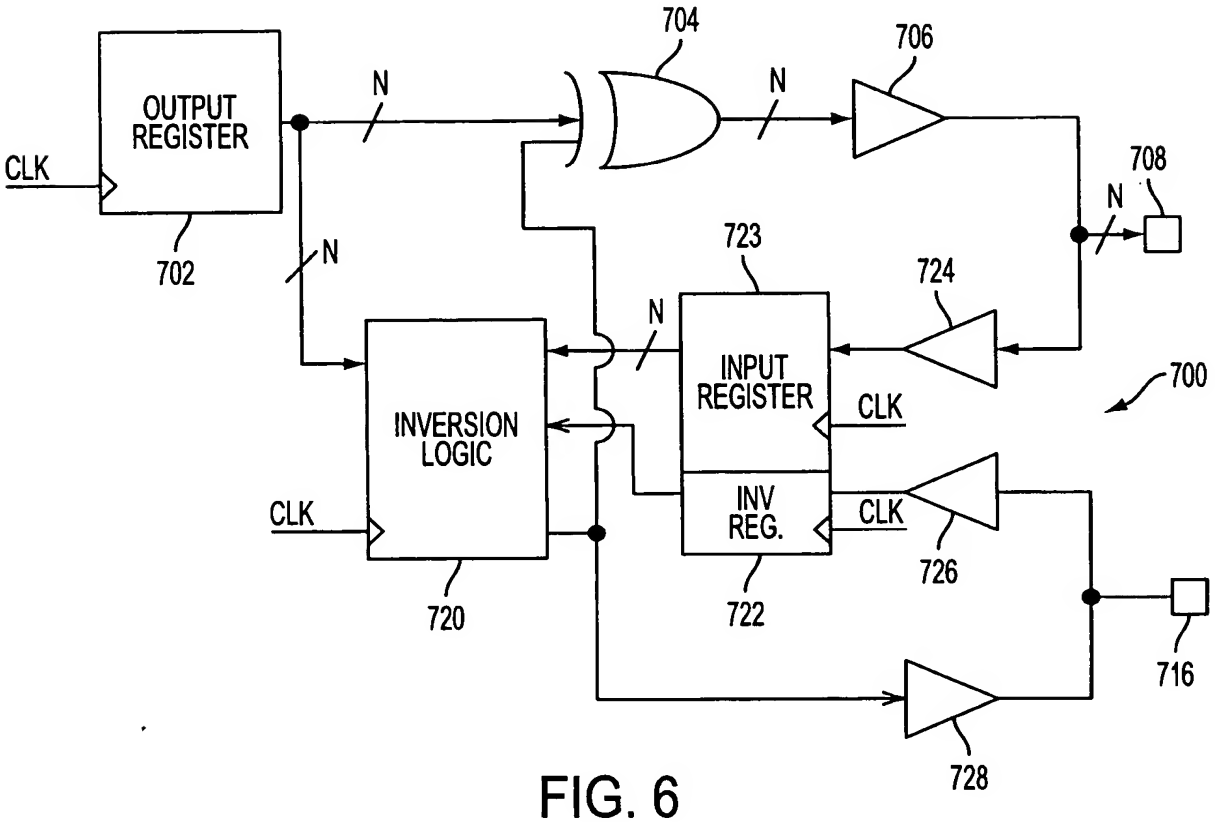
OUTPUT REGISTER
CLK
N
702
704
706
708
723
724
INPUT REGISTER
CLK
700
INVERSION LOGIC
CLK
720
INV REG.
CLK
722
726
716
728

FIG. 6

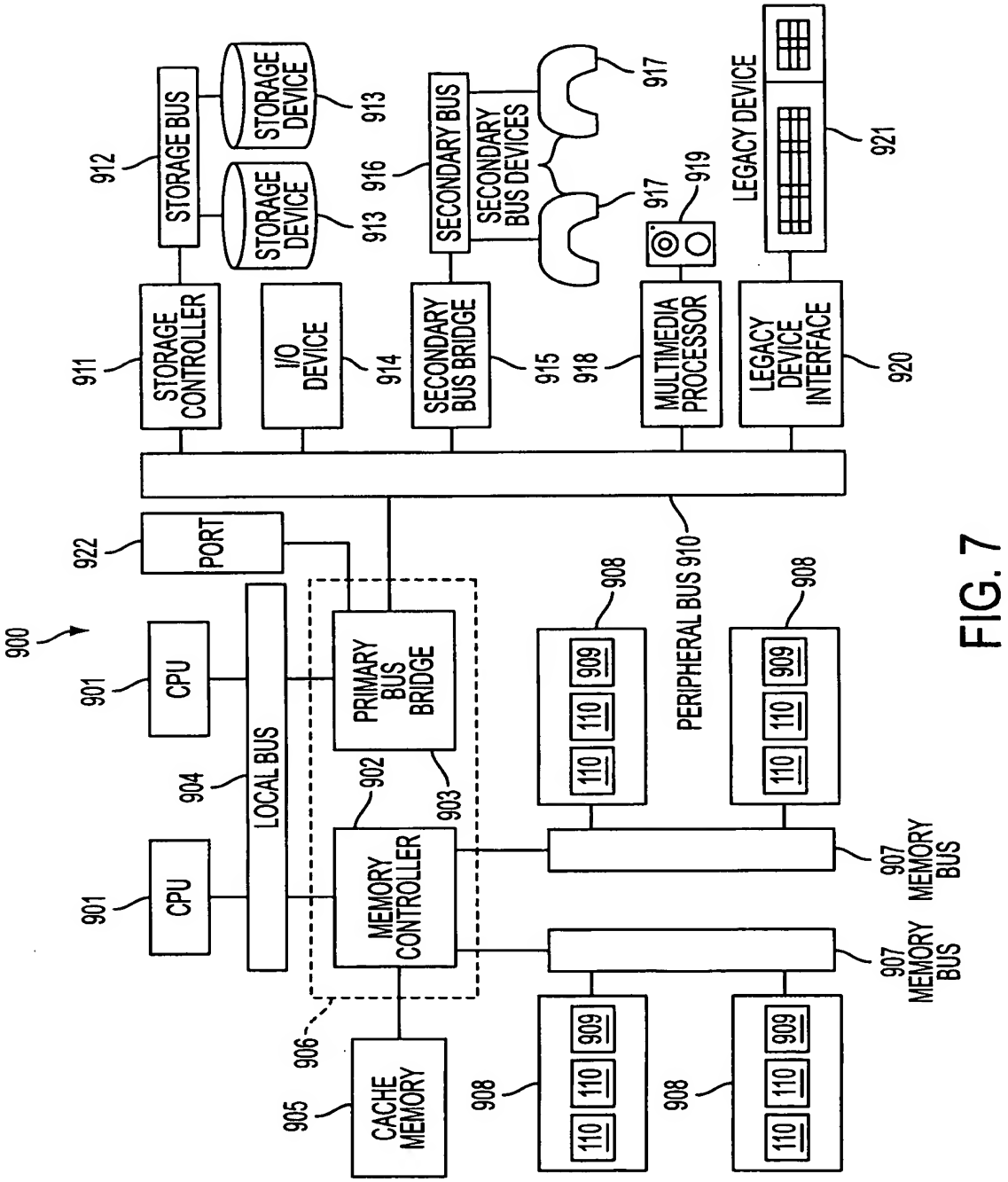
900
901
CPU
901
CPU
904
LOCAL BUS
902
903
PRIMARY BUS BRIDGE
MEMORY CONTROLLER
906
905
CACHE MEMORY
922
PORT
911
STORAGE CONTROLLER
912
STORAGE BUS
913
STORAGE DEVICE
913
STORAGE DEVICE
914
I/O DEVICE
915
SECONDARY BUS BRIDGE
916
SECONDARY BUS
917
SECONDARY BUS DEVICES
917
918
MULTIMEDIA PROCESSOR
919
920
LEGACY DEVICE INTERFACE
LEGACY DEVICE
921
PERIPHERAL BUS 910
908
909
110
907
MEMORY BUS

FIG. 7